# SOLID-STATE IMAGING DEVICE AND CAMERA INCLUDING DISCRETE TRENCH ISOLATION STRUCTURE

## CROSS REFERENCES TO RELATED APPLICATIONS

The present application is a Continuation of application Ser. No. 13/659,505, filed Oct. 24, 2012, which is a Continuation of application Ser. No. 12/003,981, filed Jan. 4, 2008, now U.S. Pat. No. 8,350,305, issued on Jan. 8, 2013, and contains subject matter related to Japanese Patent Application JP 2007-036620 filed in the Japanese Patent Office on Feb. 16, 2007, the entire contents of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a solid-state imaging device and a camera, and particularly relates to a MOS (metal-oxide semiconductor) solid-state imaging device and camera.

Description of the Related Art

Solid-state imaging devices include a charge-transfer solid-state imaging device represented by a CCD (charge-coupled device) image sensor and an amplification solid-state imaging device represented by a MOS (metal-oxide semiconductor) image sensor such as a CMOS (complementary metal-oxide semiconductor) image sensor. When comparing the CCD image sensor with the MOS image sensor, the CCD image sensor may need a high driving voltage to transfer signal electric charges, so that a power supply voltage for the CCD image sensor may be higher than that of the MOS image sensor.

Accordingly, a mobile phone unit incorporating a camera, a PDA (personal digital assistant) and other mobile devices typically use a CMOS image sensor as a solid-state imaging device mounted thereon. The CMOS image sensor is advantageous in that a power supply voltage is lower than that of the CCD image sensor and power consumption is lower than that of the CCD image sensor.

For insulating and isolating elements, a LOCOS (local oxidation of silicon) (selective oxidation) element isolation system or a STI (shallow trench isolation) element isolation system is known as an element isolation system used in the MOS image sensor (see Japanese Unexamined Patent Application Publication No. 2002-270808). In particular, the STI element isolation system has been widely used with pixels increasingly miniaturized.

In a solid-state imaging device, the number of pixels has been increased along with the resolution being improved, and a pixel is further miniaturized because the solid-state imaging device includes a large number of pixels.

## SUMMARY OF THE INVENTION

Since the pixel is increasingly miniaturized as the number thereof is increased in the MOS image sensor as described above, the area of a photodiode serving as a photoelectric conversion portion is reduced, with the result that a saturated electric charge amount and the sensitivity are reduced. Specifically, the number of electric charges photoelectrically-converted per pixel, that is, the number of electrons per pixel, is reduced and the saturated electric charge amount (accordingly, saturated signal amount) decreases. This tendency increases as the pixel is further miniaturized.



When insulation and isolation based on the LOCOS isolation system or STI isolation system is used as element isolation, a dark current and a white spot may be caused on an interface between the photodiode serving as the photoelectric conversion element and the insulated and isolated area.

It is desirable to provide a solid-state imaging device and a camera in which the sensitivity is increased by improving the conversion efficiency when converting electric charges into a signal voltage, while suppressing the occurrence of a dark current and a white spot.

According to an embodiment of the present invention, there is provided a solid-state imaging device having arrayed pixels that each include a photoelectric conversion element and a read transistor for reading electric charges photoelectrically-converted in the photoelectric conversion element to a floating diffusion portion. An element isolation region bordering the floating diffusion portion is formed of a shallow trench element isolation region, and other element isolation regions are formed of an impurity diffusion isolation region.

According to an embodiment of the solid-state imaging device and the camera of the present invention, since the element isolation region bordering the floating diffusion portion is formed of the shallow trench element isolation region, the capacity of the floating diffusion portion is reduced, so that the conversion efficiency is increased. Since other element isolation regions are formed of the impurity diffusion isolation region, the occurrence of a dark current and a white spot can be suppressed.

According to the embodiment of the solid state imaging device and the camera of the present invention, it is possible to increase the sensitivity by improving the conversion efficiency while suppressing a dark current and a white spot. Accordingly, the solid-state imaging device and the camera of the embodiment are suitable for application to the solid-state imaging device and the camera in which the area of a pixel is reduced as the number of pixels is increased.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram showing an example of an arrangement of a MOS image sensor to which an embodiment of the present invention is applied.

FIG. **2** is a circuit diagram showing an example of a circuit arrangement of a unit pixel.

FIG. **3** is a circuit diagram showing another example of a circuit arrangement of a unit pixel.

FIG. **4** is a diagram showing a solid-state imaging device according to a first embodiment of the present invention, in particular, showing main portions of a pixel array portion thereof.

FIG. **5** is a cross-sectional view on the line D-D shown in FIG. **4**.

FIG. **6** is a diagram showing main portions of the unit pixel shown in FIG. **4** in an enlarged-scale.

FIG. **7**A is a cross-sectional view on the line A-A in FIG. **4**; FIG. **7**B is a cross-sectional view on the line B-B in FIG. **4**; and FIG. **7**C is a cross-sectional view on the line C-C in FIG. **4**.

FIGS. **8**A and **8**B are a plan view and a cross-sectional view respectively showing an example of a gate electrode of a pixel transistor.

FIGS. **9**A and **9**B are a plan view and a cross-sectional view respectively showing another example of a gate electrode of a pixel transistor.